FIG.1

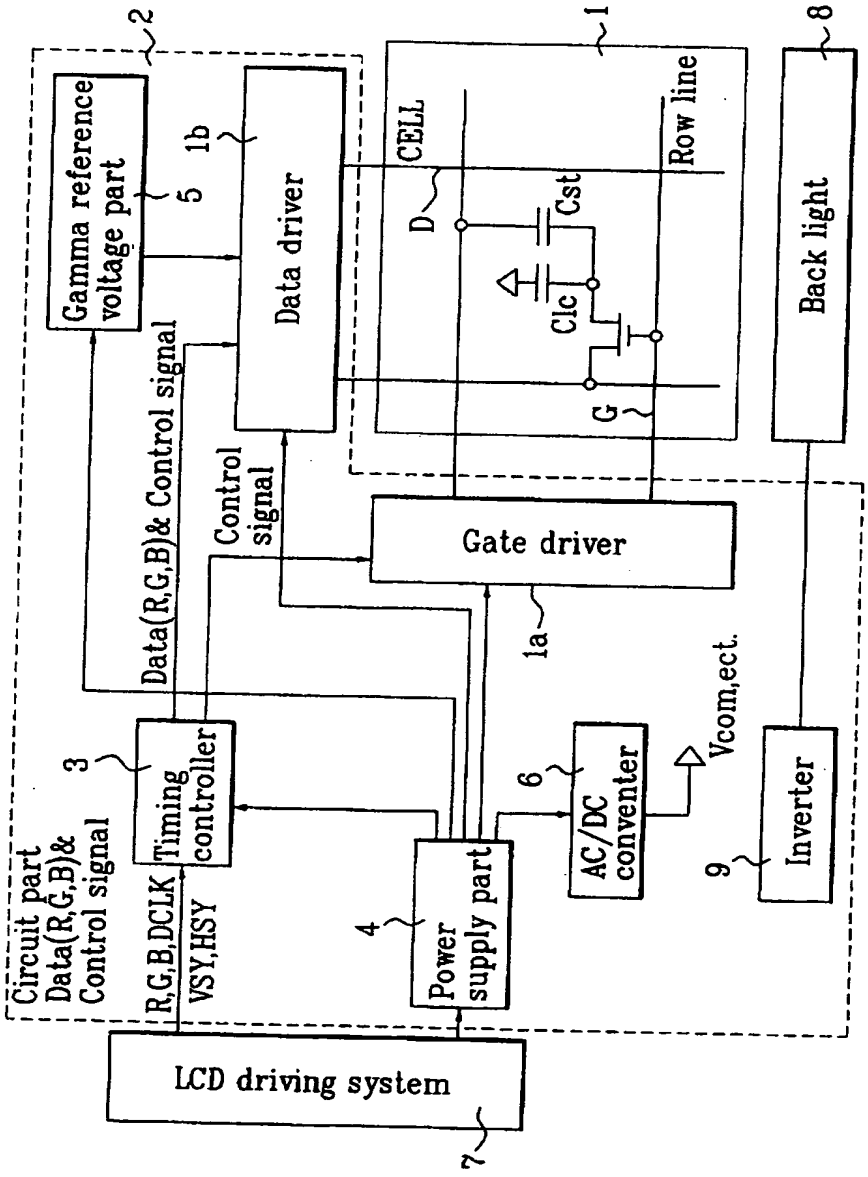

2
Gamma reference voltage part
5
1b
Data driver
1
CELL
D
Cst
Clc
G
Row line
8
Back light
Data(R,G,B)& Control signal
Control signal
Gate driver
1a
Circuit part
Data(R,G,B)&
Control signal
3
Timing controller
R,G,B,DCLK
VSY,HSY
4
Power supply part
6
AC/DC conventer
Vcom,ect.
9
Inverter
LCD driving system
7

FIG.2
Related Art

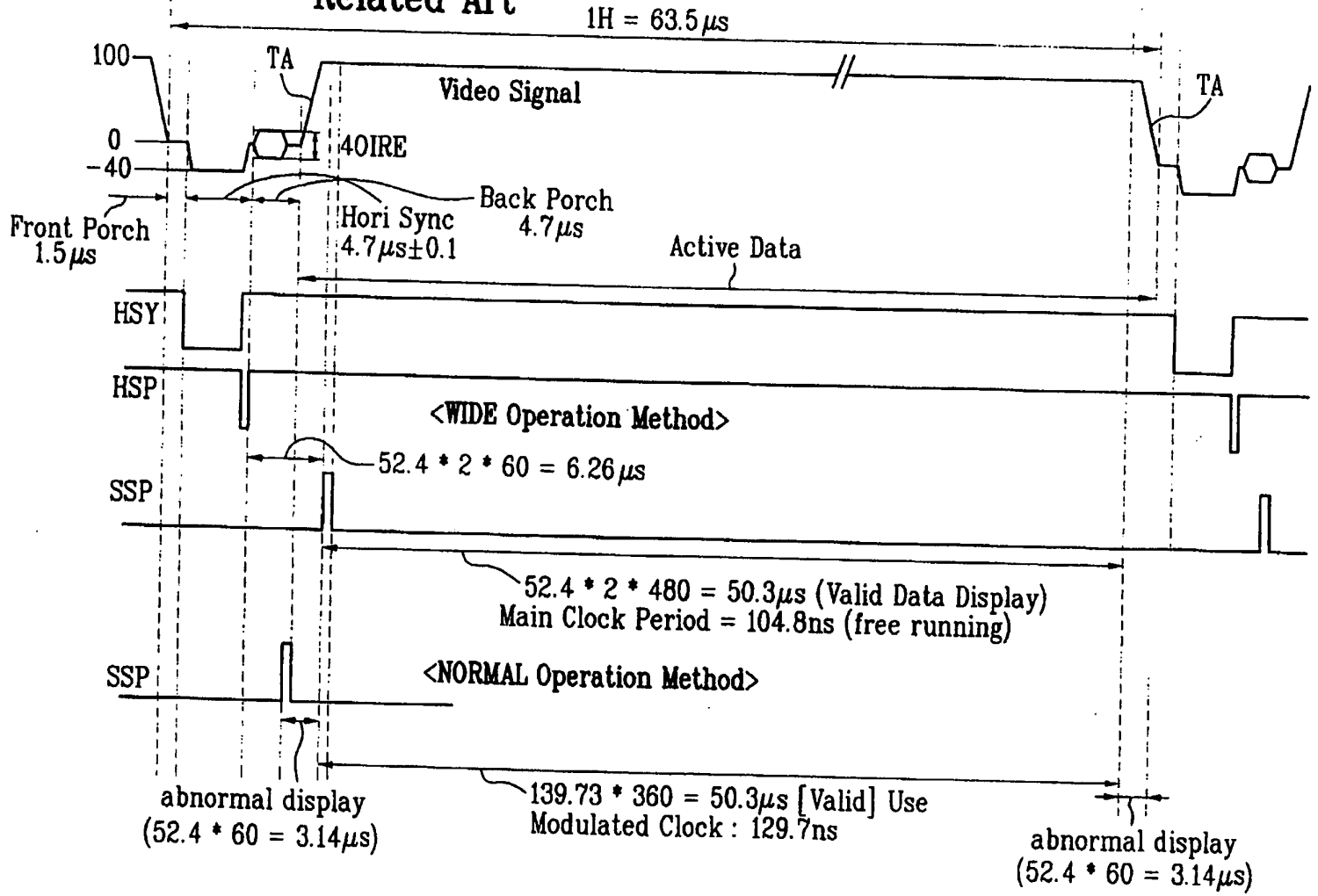
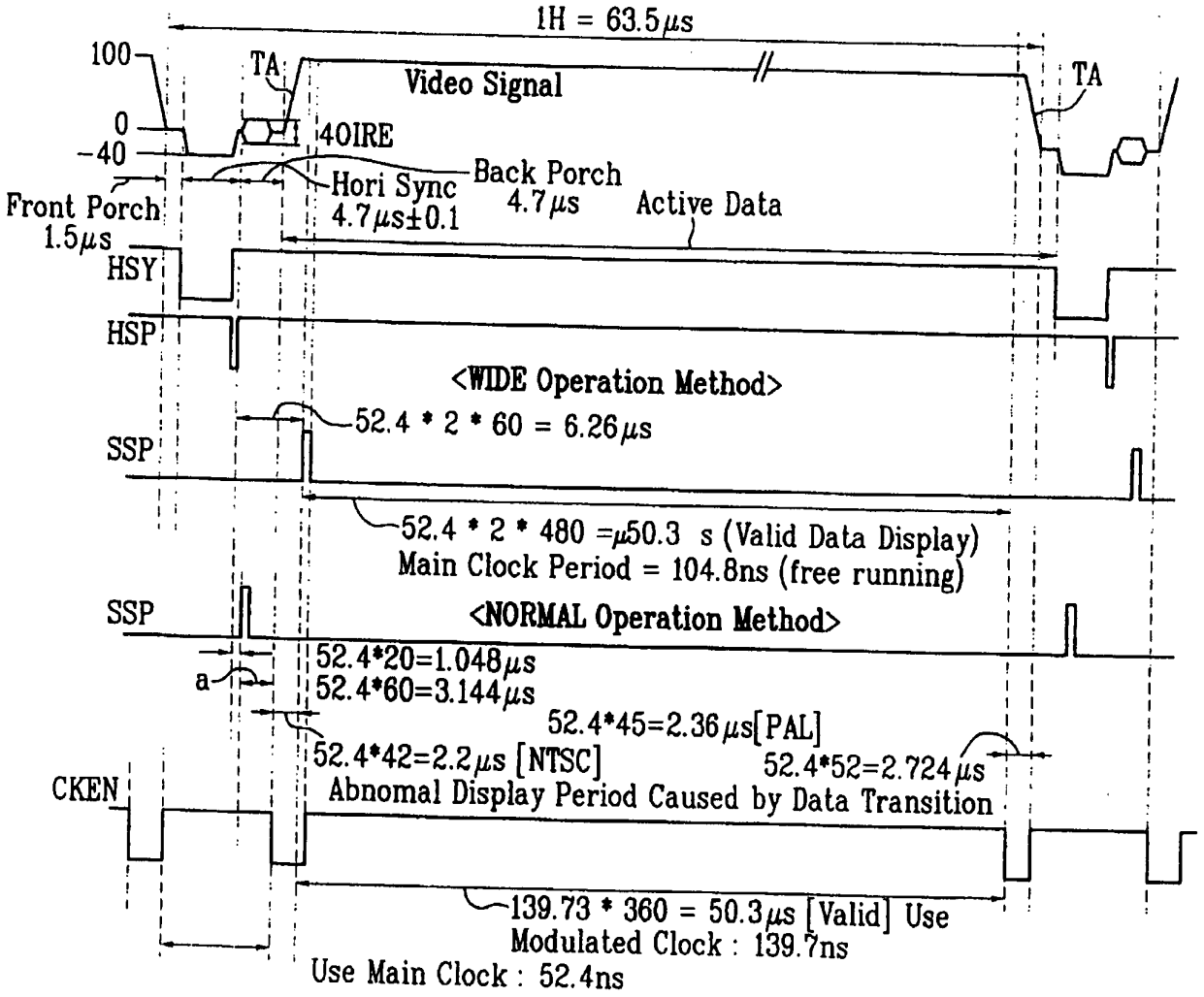


FIG.3


1H = 63.5μs
100
0
-40
TA
Video Signal
40IRE
TA
Front Porch
1.5μs
Hori Sync
4.7μs±0.1
Back Porch
4.7μs
Active Data
HSY
HSP
<WIDE Operation Method>
52.4 * 2 * 60 = 6.26μs
SSP
52.4 * 2 * 480 =μ50.3 s (Valid Data Display)
Main Clock Period = 104.8ns (free running)
SSP
<NORMAL Operation Method>
52.4*20=1.048μs
a
52.4*60=3.144μs
52.4*45=2.36μs[PAL]
52.4*42=2.2μs [NTSC]
52.4*52=2.724μs
CKEN
Abnomal Display Period Caused by Data Transition
139.73 * 360 = 50.3μs [Valid] Use
Modulated Clock : 139.7ns
Use Main Clock : 52.4ns